What is Claimed is:

1. A system for connecting a set of device chips by means of an array of microjoint structures on an interconnect carrier comprising:

the carrier including a multilayer substrate having a plurality of microjoint receptacles in one surface.

a set of microjoint pads, including solder balls, on the device chips joined to the receptacles in the one carrier surface,

interconnect wiring mounted in the carrier connecting to the microjoint pad arrays to enable the interconnection between device chips mounted on the carrier.

2. A system as defined in Claim 1, wherein said receptacles on said interconnect carrier comprise successive layers of a liner layer, seed layer, barrier layer and a noble metal layer, respectively, these layers lining the inner surface of said receptacles.

3. A system as defined in Claim 2, wherein the liner layer is selected from the group consisting of Ta, TaN, Ti, TiN, W, WN, Cr and combination thereof.

4. A system as defined in Claim 3, wherein the liner layer thickness is between 50A and 1200A.

5. A system as defined in Claim 2, wherein the seed layer is copper with thickness in the range 300A to 2000A.

6. A system as defined in Claim 2, wherein the barrier layer is selected from the group consisting of Ni, Co, Pt, Pd and alloys or combinations thereof.

7. A system as defined in Claim 6 wherein the barrier layer thickness is between 1000A and 10,000A.

8. A system as defined in Claim 1 wherein said microjoint pads on said device chips comprise successive layers of a liner layer, seed layer, barrier layer and a fusible solder layer, respectively.

9. A system as defined in Claim 8 wherein the liner layer is selected from the group comprising Ta, TaN, Ti, TiN, W, WN, Cr and combinations thereof..

10. A system as defined in Claim 8 wherein the seed layer is copper with thickness in the range 300A to 2000A.

11. A system as defined in Claim 8 wherein the barrier layer is selected from the group comprising Ni, Co, Pt, Pd and alloys or combinations thereof.

12. A system in accordance with Claim 11 wherein the barrier layer thickness is between 1000A and 10,000A.

13. A system as defined in Claim 2 wherein the carrier is made of silicon and includes a set of interconnect wiring disposed thereon, a dielectric passivation layer over the top surface of the interconnect wiring and said receptacles being in the dielectric passivation layer.

14. A system as defined in Claim 12 wherein the device chiplet includes a set of devices built on it connected by wiring, a dielectric passivation layer over the top surface of the wiring and said microjoint pads being in the dielectric passivation layer.

15. A system as defined in Claim 12 wherein the device chiplets are selected from the group comprising microprocessor chip, memory chip, microcontroller chip, laser diode chip, laser driver chip, photodetector chip, wireless communication chip, and logic processor chip.

16. A microjoint interconnect structure comprising:

(a) a carrier substrate having an array of interconnects for connecting device components;

(b) the carrier, including a substrate and a dielectric film, and microjoint receptacles comprising an adhesion layer, diffusion barrier layer and a noble metal layer.

(c) microjoining pads on the device side, comprising an adhesion layer, solder reaction barrier layer and fusible solder joint ball for each component

(d) said microjoint pads on the device on the carrier side matching said microjoint receptacles on the carrier side.

17. A microjoint interconnect structure as defined in Claim 16 wherein the device components are semiconductor chips, optical component chips and the like.

18. A process for connecting a set of device chips by means of an array of microjoint structures on an interconnect carrier comprising:

forming the carrier including a multilayer substrate having a plurality of microjoint receptacles in one surface.

forming a set of microjoint pads, including solder balls, on the device chips joined to the receptacles in the one carrier surface,

forming interconnect wiring mounted in the carrier connecting to the microjoint pad arrays to enable the interconnection between device chips mounted on the carrier.

19. A microjoint interconnect structure comprising:

(a) a carrier substrate having an array of interconnects for connecting device components.

(b) the carrier, including a substrate and dielectric film with microjoining pads each comprising an adhesion layer, solder reaction barrier layers and fusible solder joint ball.

(c) the microjoint receptacles on the device side comprising an adhesion layer, diffusion barrier layer and a noble metal layer.

(d) said microjoint pads on the carrier side matching said microjoint receptacles on the device.

20. A microjoint interconnect structure as defined in Claim 19 wherein the device chips are selected from the group comprising semiconductor chips, optical device chips, communication chips.

21. A process for connecting a set of device chips by means of an array of microjoint structures on an interconnect carrier comprising:

forming the carrier including a multilayer substrate having a plurality of microjoint pads including solder balls on one surface.

forming a set of microjoint receptacles on one surface of the device chips that are joined to the carrier by the solder balls on the carrier.

forming interconnect wiring on the carrier connecting the microjoint pad arrays to enable the interconnection between the chips.